REMARKS

Claims 1-3, 18-21, 37-53, and 58-64 are pending in the subject application. Claims 1 and 18 have been amended by the present amendment. The amendments are fully supported by the specification as originally filed. Applicants' remarks in the response filed on October 14, 2003 are incorporated by reference herein.

Applicants' invention is exemplified by the latch circuit diagram of FIG. 3. As shown in FIG. 3, latch circuit LAT includes clock signal input control sections 12 and 13 for inputting a clock signal ck (/ck) and a pulse signal in (/in), where the clock signal has an amplitude smaller than an amplitude of the pulse signal. For example, in the embodiment of FIGS. 1-4, the clock signal is 5 V and the pulse signal is 16 V.

Claims 1-3, 18, 37, 62 and 64 were rejected under obviousness-type double patenting as being unpatentable over claims 1 and 15 of U.S. Patent 6,580,411. The double patenting rejection is respectfully traversed in view of the amendments and remarks contained herein.

Claims 1-3, 18-21, 37, 53, 58, and 59 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 6,166,725 to Isami et al. (hereinafter "Isami"). This rejection is respectfully traversed.

In the Office Action, FIGS. 1-5 of Isami were cited for allegedly teaching:

> a [first] input signal, which is a data pulse signal using data bus 233, and a second input signal, which is a clock pulse signal D2 (a data latch clock D2) for the latch circuit 165 producing an output pulse signal, whose signal could be shifted for having a bigger amplitude than the input pulse signal using the level shifter (Office Action, page 3, paragraph 4).

Regarding the "first input signal" cited in the Office Action, it was stated that an image data signal transmitted through a data bus 233 of Isami (see FIG. 4) is input to a latch circuit. However, Isami fails to teach or suggest a pulse signal for latching image data which is input into a latch circuit. In Isami, image data is transmitted via the data bus 233 into a latch circuit. In contrast, the Applicants' claimed invention provides that pulse signals for latching image data are input to the latch circuit LAT, whereas the image data itself is never input to the latch circuit LAT (see FIG. 1 of application).

Regarding the "second input signal" cited above, it was alleged that the pulse signal output from the latch circuit 165 of FIG. 1 (where FIG. 1 of Isami is a detailed drawing of the drain driver 230 of FIG. 4) is amplified by the level shifter 156. As shown in FIG. 1, a latch control signal is transmitted horizontally with constant amplitude through the row of latches, whereas the image data signal is sampled by the latch circuit 165 and transmitted vertically downward to the level shifter 156. However, the image data signal of Isami does not correspond to the pulse signal recited in the Applicants' claimed invention. As explained in the Applicants' specification, the "pulse signal" in the Applicants' invention refers to an output signal OUT from a latch circuit whose amplitude is greater than a clock signal ck. Therefore, the image data signal sampled by the latch circuit 165, as taught in Isami, does not correspond to the "pulse signal" recited in claims 1, 18, and 37.

In the Office Action, it was further alleged that although Isami does not expressly teach a clock signal having an amplitude smaller than the amplitude of the "pulse signal," it would have been obvious "to use small amplitude input signals, which are level shifted and/or amplified later" (Office Action, page 4, first paragraph). However, the above observation can only be made with the benefit of hindsight reasoning. Moreover, by applying this reasoning to Isami, the signals D2 input to the latch circuit 165 would be level shifted upon reaching the level shifters 156. However, as discussed above, only the image data signals (not the clock signals D2) are transmitted vertically downward, and thus level shifted, by the level shifters 156. The clock signals D2 are transmitted horizontally through the row of latches 165, and thus would not be

level shifted in Isami. Therefore, the proposed level shifting or amplification of a clock signal simply could not occur in the Isami reference.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Applicants believe that additional fees are not required for consideration of the within Amendment. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,

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